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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,061	07/18/2003	Stephan Gehring	30287-93	3982

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EXAMINER	
SHAH, CHIRAG G	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,061	GEHRING ET AL.	
	Examiner	Art Unit	
	Chirag G. Shah	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-14 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 respectively of copending Application No. 09/480,837. Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicants claim 1 merely broadens the scope of patent application number 09/480,837 by eliminating "ultra wide band network" and "ultra wide band pulses". It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA). Also note Ex Parte Raine, 168 USPQ 3.75 (bd. APP. 1969) ; omission of a reference element whose function is not needed would have been obvious to one skilled in the art.

The comparison of two applications

Regarding claims 1 and 14 [similar to claim 1 and 14 respectively of copending Application No. 09/480,837, except broader by eliminating ultra wide band network" and "ultra wide band pulses"].

Regarding claim 2-13 and 15-16 [similar to claim 2-13 and 15-16 respectively of copending Application No. 09/480,837].

3. Claims 1-4, 8-9, 13-14 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12-16 of copending Application No. 10/611,199. Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicants claim 1 merely broadens the scope of patent application number 10/611,199 by eliminating "ultra wide band network" and "ultra wide band pulses". It has been held that the omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA). Also note Ex Parte Raine, 168 USPQ 3.75 (bd. APP. 1969) ; omission of a reference element whose function is not needed would have been obvious to one skilled in the art.

The comparison of two applications:

Regarding claims 1, 9 and 14 [similar to claim 12 of copending Application No. 10/611,199, except broader by eliminating ultra wide band network" and "ultra wide band pulses" and narrower by adding "timestamp slot" and "synchronization slot"].

Regarding claim 2, [identical to claim 13 of copending Application No. 10/611,199].

Regarding claim 3, [identical to claim 14 of copending Application No. 10/611,199].

Regarding claims 4 and 13, [identical to claim 15 of copending Application No. 10/611,199].

Regarding claim 8, [identical to claim 16 of copending Application No. 10/611,199].

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-7 and 9-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello et al. (U.S. Patent No. 6,275,544) in view of Hulyalkar (U.S. Patent No. 6,347,084).

Regarding claims 1 and 9, Aiello discloses in **fig. 1 and col. 7, lines 47-67** of (an ultra wide band) network having a master device **[device 12a, fig. 1 and col. 5, lines 45-61]** and a plurality of slave devices **[12b and 12c, see fig. 1 and col. 5, lines 45-61]** in network communication with the master device (using a plurality of ultra wide band pulses) **[the master transceiver performs data transmission between several node devices via a MAC protocol utilizing a TDMA fame definition. Under the TDMA architecture, the data transmitted as short RF pulses divided into discrete data frames; see col. 7, lines 47-67]**, a Medium Access Control layer protocol for transmission and reception of network packets **[see col. 7, lines 47-67]**, comprising:

a Time Division Multiple Access frame definition **[see fig. 3 and col. 7, lines 47-55]** having a start-of-frame section **[SOF, see col. 7, lines 65-67]**, a command section **[command slot 42, see fig. 3]**, a data slot section containing a plurality of variable length slots **[see col. 8, lines 45-59 and fig. 3]**, a synchronization slot **[master sync code 46, see col. 8, lines 1-21 and fig. 3]**.

Aiello fails to disclose of a TDMA frame including a timestamp slot. Hulyalkar teaches a method of timestamp synchronization that includes a control node (master device) and a plurality of other nodes (slave devices) that are in communication with one another mediated by a MAC subsystem that uses a reservation-based TDMA protocol. Hulyalkar discloses in col. 5, lines 5-17 and col. 9, lines 41-65 and respective portion of the specification to include a control node sending a preset command to slave nodes and it presets their respective timestamp to the prescribed timestamp value. Thus, having a timeslot within a TDMA frame. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to incorporate the teachings of a timestamp timeslot within a TDMA frame as taught by Hulyalkar into Aiello invention. One is motivated as such in order to enable permit precise, deterministic scheduling with reduction in delay and processing time for a reservation-based TDMA protocol.

Regarding claim 14, Aiello discloses a method for scheduling the assignment of variable length data **[see col. 8, lines 45-59 and fig. 3]** slots in network having a master device **[device 12a , fig. 1 and col. 5, lines 45-61]** and a plurality of slave devices **[12b and 12c, see fig. 1 and col. 5, lines 45-61]** in network communication with the master device (using a plurality of ultra wide band pulses) **[the master transceiver performs data transmission between several node**

devices via a MAC protocol utilizing a TDMA fame definition. Under the TDMA architecture, the data transmitted as short RF pulses divided into discrete data frames; see col. 7, lines 47-67], comprising:

providing Time Division Multiple Access frame definition **[see fig. 3 and col. 7, lines 47-55]** having a start-of-frame section **[SOF, see col. 7, lines 65-67]**, a command section **[command slot 42, see fig. 3]**, a data slot section containing a plurality of variable length slots **[see col. 8, lines 45-59 and fig. 3]**, a synchronization slot **[master sync code 46, see col. 8, lines 1-21 and fig. 3]**; and

determining a schedule time to communicate the assignment and reallocation of said variable-length data slots to each of said slave devices **[Aiello discloses in col. 7, lines 47-67 and in col. 8, lines 45-60, wherein the MAC layer protocol is configured to implement dynamic requisition, allocation, and reallocation of variable length data slots within the frame and further discloses in figs. 1, 3, col. 5, lines 62-67 and col. 8, lines 45-59, wherein said master device and slave device are further configured to coordinate a scheduled switch from a first set of data slot parameters to second set of data slot parameters].**

Aiello fails to disclose of a TDMA frame including a timestamp slot. Hulyalkar teaches a method of timestamp synchronization that includes a control node (master device) and a plurality of other nodes (slave devices) that are in communication with one another mediated by a MAC subsystem that uses a reservation-based TDMA protocol. Hulyalkar discloses in col. 5, lines 5-17 and col. 9, lines 41-65 and respective portion of the specification to include a control node sending a preset command to slave nodes and it presets their respective timestamp to the prescribed timestamp value. Thus, having a timeslot within a TDMA frame. Therefore, it would

have been obvious to one of ordinary skills in the art at the time of the invention to incorporate the teachings of a timestamp timeslot within a TDMA frame as taught by Hulyalkar into Aiello invention. One is motivated as such in order to enable permit precise, deterministic scheduling with reduction in delay and processing time for a reservation-based TDMA protocol.

Regarding claims 2-4 and 13, Aiello discloses in col. 7, lines 47-67 and in col. 8, lines 45-60wherein the MAC layer protocol is configured to implement dynamic requisition, allocation, and reallocation of variable length data slots within the frame.

Regarding claims 5, 12, and 15-16, Aiello discloses in figs. 1, 3, col. 5, lines 62-67 and col. 8, lines 45-59, wherein said master device and slave device are further configured to coordinate a scheduled switch from a first set of data slot parameters to second set of data slot parameters as claim.

Regarding claim 6 and 10, Aiello fails to disclose further comprising a bit-field which is configured to be incremented by the master device in a modulo-N manner by a which is incremented by a master timestamp counter within the timestamp slot of data slot parameters. Hulyalkar discloses in claims 7 and 11 and respective portions of the specification of comparing timestamp counter value in each nodes (slave). Hulyalkar also disclose a timestamp register and counter that includes a bit-field for incrementing. Hulyalkar further discloses in the above disclosed sections that includes comparator that compares the timestamp values stored and coordinates switch from a first set of data slot to a second set of data slot at different times.

Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings at the time of the invention to include the teachings of Hulyalkar in order to precisely determine timing for the entire system and execute transmission with minimal delay or packet loss.

Regarding claims 7 and 11, Aiello fails to disclose wherein each of said slave devices is configured to maintain a local copy of said master timestamp counter. Hulyalkar discloses in claims 7 and 11 and respective portions of the specification of comparing timestamp counter value in each nodes (slave), thus suggesting each of the slave devices is configured to maintain a copy of the master counter. Hulyalkar also disclose a timestamp register and counter that includes a bit-field for incrementing. Hulyalkar further discloses in the above disclosed sections that includes comparator that compares the timestamp values stored and coordinates switch from a first set of data slot to a second set of data slot at different times. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings at the time of the invention to include the teachings of Hulyalkar in order to precisely determine timing for the entire system and execute transmission with minimal delay or packet loss.

5. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello et al. (U.S. Patent No. 6,275,544) in view of Hulyalkar (U.S. Patent No. 6,347,084) as applied above, and further in view of Kadambi et al. (U.S. Patent No. 6560229), hereinafter Kadambi.

Regarding claim 8, Aiello in view of Hulyalkar fails to disclose wherein said variable-length data slots of said frame have a granularity of one bit. Kadambi discloses col. 8, lines 50 to col. 9, lines 6 that the MAC layer protocol as recited, wherein variable length data slots of frame

have a granularity of one bit as claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Aiello in view of Hulyalkar to include the teaching of Kadambi in order to provide a reservation scheme for data traffic and a random access technique for control and signaling traffic.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7682. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

cgs
December 13, 2006

Chirag Shah
Primary Examiner, 2616

CHIRAG G. SHAH
PRIMARY PATENT EXAMINER